



2026.3 Release Highlights

- ☐ UltraCore updates
- ☐ Software performance improvements
- ☐ IP protection updates
- ☐ HV Source component
- ☐ Grid Modernization communication updates
- ☐ UX improvements



UltraCore updates

Simulate more converters with UltraCore solver resolution

❑ Modularized UltraCore solver

- Up to 3 converter topologies can be simulated within a single UltraCore unit
- Each converter supported by UltraCore has a defined

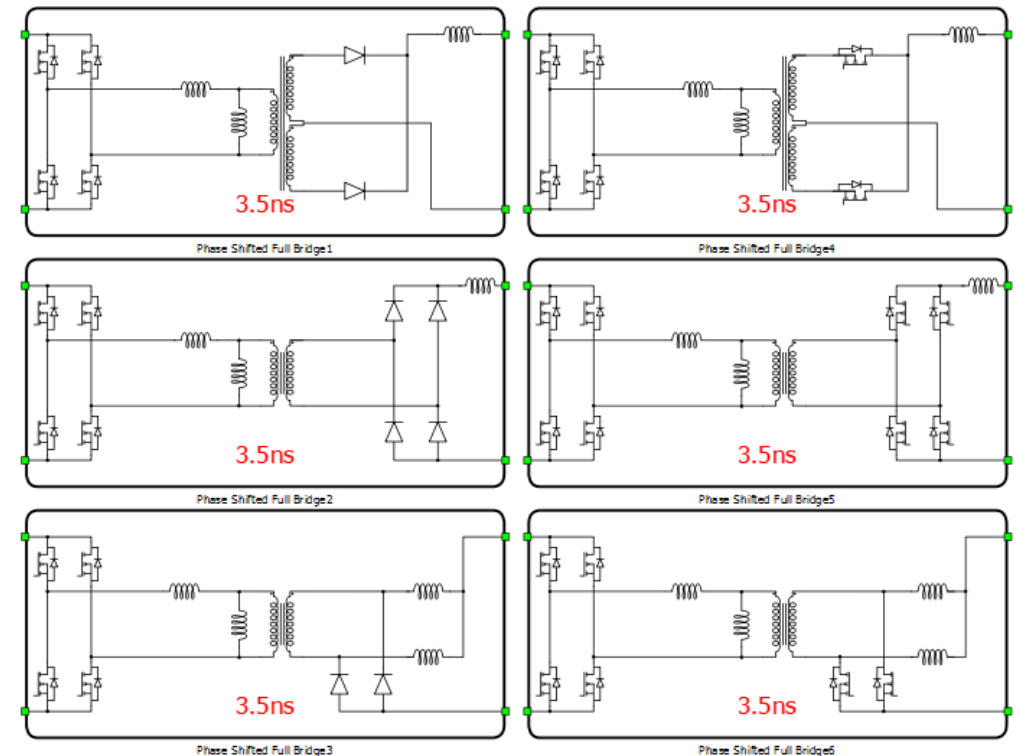
UltraCore weight parameter:

- ❑ Dual Active Bridge: **1**
- ❑ Resonant Converter: **3**

❑ New topology - Phase Shifted Full Bridge (PSFB)

- 6 different variations
- UltraCore weight: **3**

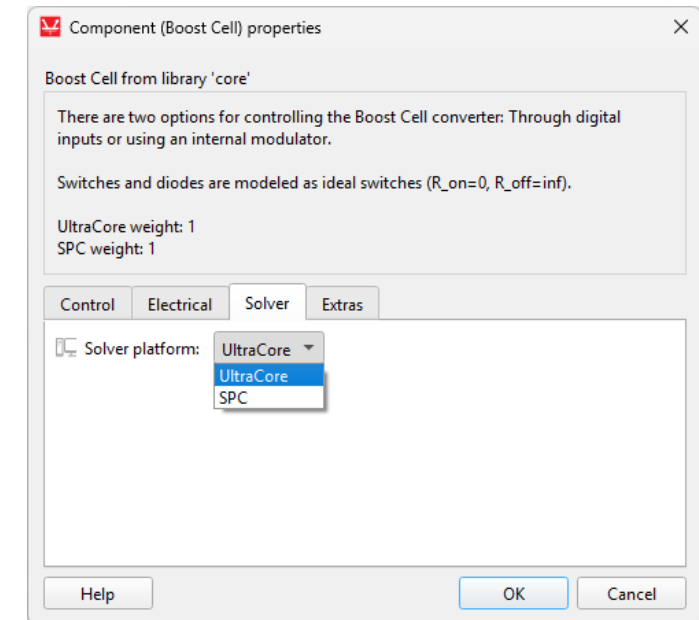
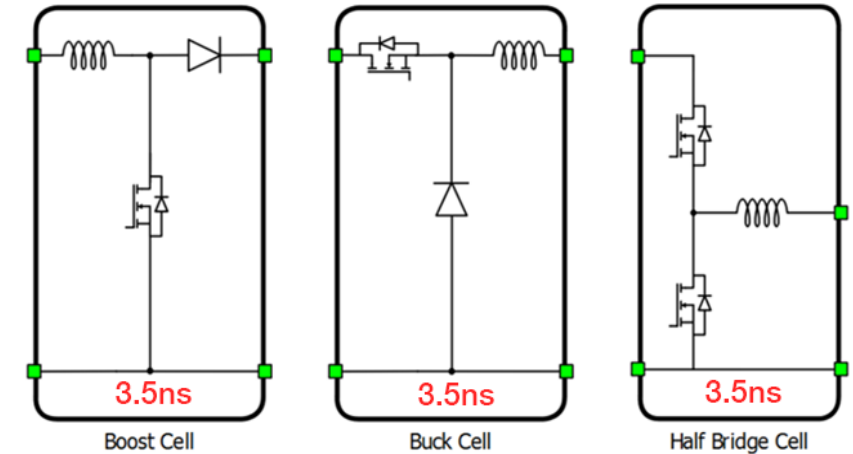
```
Running Device specific hw utilization analysis:
Standard processing core utilization: 1 out of 2 50.0%
MachineCores utilization: 0 out of 1 0.0%
UltraCores utilization: 2 out of 2 100.0%
  UltraCore0 weight utilization: 3 out of 3 100.0%
  UltraCore1 weight utilization: 2 out of 3 66.67%
Signal generator utilization: 3 out of 12 25.0%
Look up tables utilization: 0 out of 8 0.0%
PWM modulator utilization: 0 out of 12 0.0%
PWM analyzer utilization: 0 out of 0 0.0%
Parallel DTV Conv. Detectors utilization: 0 out of 3 0.0%
```



UltraCore updates

Simulate more converters with UltraCore solver resolution

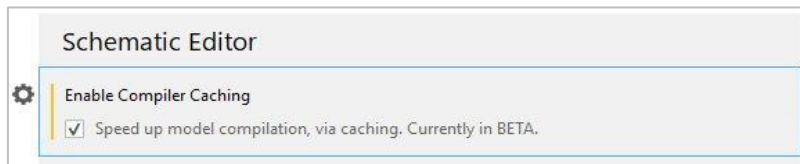
- New converter topologies supported:
 - Boost Cell
 - Buck Cell
 - Half Bridge Cell
- Solver flexibility
 - Quickly switch between UltraCore solver and Standard Processing Core (SPC) solver
 - Validate different solver options while keeping the same topology underneath
- Efficiency
 - Up to 3 converters simulated on a single UltraCore unit
 - UltraCore weight: **1**



Software performance improvements

Increased user productivity with new performance improvements

- ❑ Model compiling caching
 - Compiler caches previously compiled parts of the model
 - Skips electrical model (PE) compilation if changes only affect signal processing elements
 - Skips signal processing (SP) compilation if changes only affect electrical model elements
 - Skip unchanged partitions of the model in multi-HIL models
 - Comes disabled by default in THCC settings



```
Checking component connections...
Resolving the schematic model...
Evaluating the properties of the components...
Checking component types...
Model is divided into 2 sub-models
Validation passed!
Compiling process started (2026-07-21 18:52:04), please wait...
Device id 0 model unchanged. Compilation skipped.

-----h11-----
Compiling model for device with id 1

PWM Modulators scheduling completed.

Device id 1 PE part unchanged. Compilation skipped.

Allocating IO resources for user 0 CPU...
Signal processing Scada Input utilization:      0 out of 104
Signal processing Scada Output utilization:     0 out of 104
Signal processing Comm parameters utilization:  0 out of 838
Signal processing Probes utilization:           1 out of 102
Signal processing Digital Probes utilization:   0 out of 512
Signal processing tunable parameters utilization: 0 out of 262

Starting code generation for user 0 CPU...
C code generated successfully!
Starting compilation of generated C code...
Total utilization of the external memory:      1591 out of 65536
Code segment size:                            41 out of 65536
Data segment size:                           1549 out of 65536
C code compilation was successful!

Compiling model for device with id 1 finished successfully

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Compilation finished successfully.
Compiling process finished (2026-07-21 18:52:09). Duration: 5.5s.
```

Software performance improvements

Increased user productivity with new performance improvements

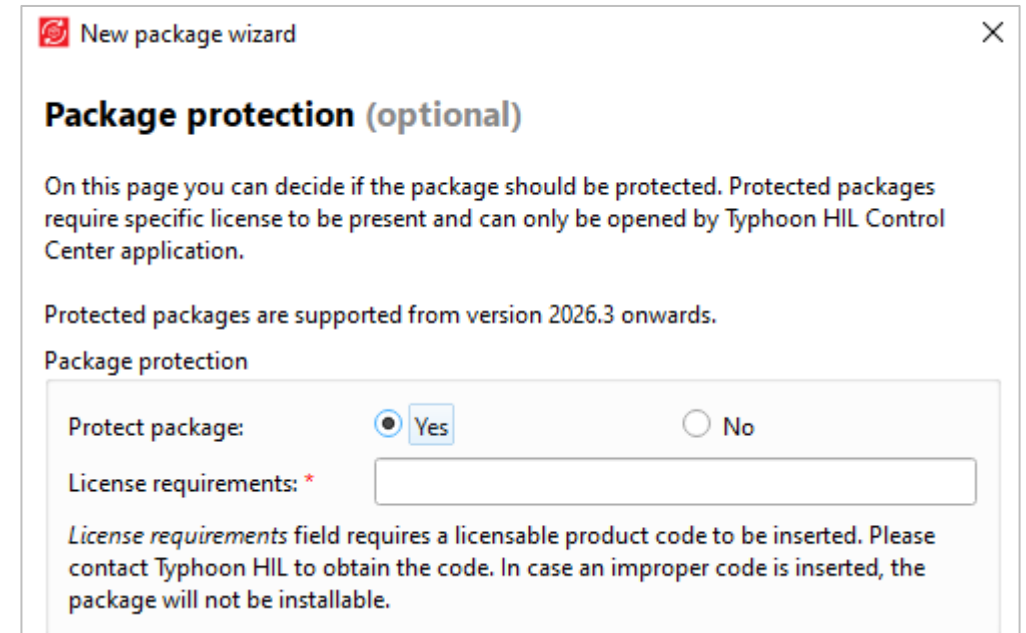
- TyphoonSim simulation start and preparation times significantly reduced
 - Removed per-run process startup overhead
 - Applies to both GUI and API based simulation

- Reduced discrete state space calculation time during model compilation
 - Enabled parallelization for large numbers of circuit modes in electrical models
 - Especially noticeable when compiling models with HILCore configurations with more matrix memory, or for VHIL+

IP protection updates

Limit package access to those with appropriate licenses

- ☐ New **Package protection** option in the **New package wizard** tool
- ☐ Select **Protect package** and assign specific **License requirements**
- ☐ Only users that have a license with the mentioned requirements can install and use the package



The screenshot shows a 'New package wizard' window with a close button (X) in the top right corner. The title bar reads 'New package wizard'. The main heading is 'Package protection (optional)'. Below this, a paragraph explains: 'On this page you can decide if the package should be protected. Protected packages require specific license to be present and can only be opened by Typhoon HIL Control Center application.' Another paragraph states: 'Protected packages are supported from version 2026.3 onwards.' The section 'Package protection' contains a 'Protect package:' label with two radio buttons: 'Yes' (selected) and 'No'. Below this is a 'License requirements: *' label followed by an empty text input field. A note at the bottom reads: 'License requirements field requires a licensable product code to be inserted. Please contact Typhoon HIL to obtain the code. In case an improper code is inserted, the package will not be installable.'

IP protection updates

Support for hard-locked components

- New **Hard-locked** component option in the **Requirements** tab:
 - **When unchecked:** If the requirement expression is not satisfied, the model cannot run, but the component implementation remains visible
 - **When checked:** If the requirement expression is not satisfied, both the model functionality and the component implementation are inaccessible

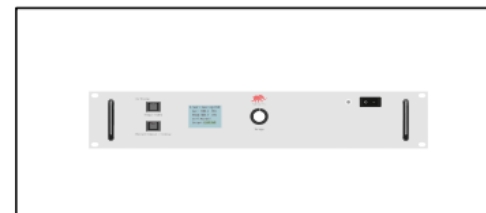


The screenshot shows a software interface with three tabs: 'Builder', 'Handlers', and 'Requirements'. The 'Requirements' tab is active. Below the tabs is a section titled 'Component visibility and requirements'. It contains two text input fields: 'Visibility' with the placeholder text 'Enter component visibility', and 'Requirement' with the text 'tb_something'. Below these fields is a checkbox labeled 'Hard-locked' which is checked, indicated by a checkmark in a box. The 'Hard-locked' checkbox and its label are highlighted with a red rectangular border.

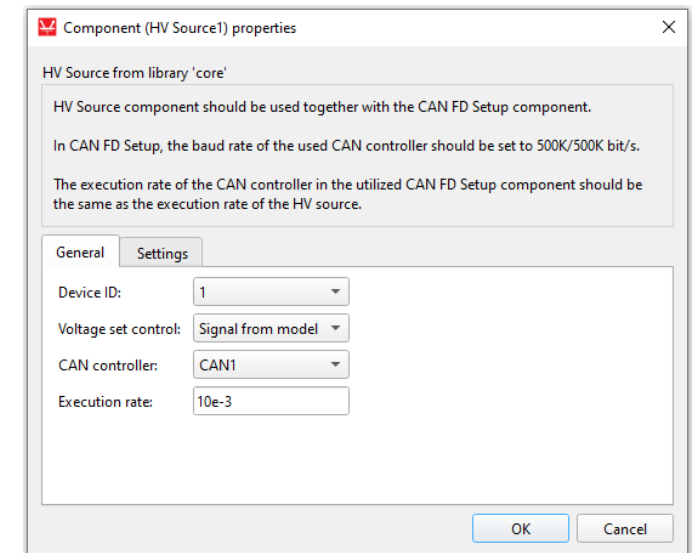
HV Source component

New addition to the HIL interfaces library

- ❑ Component used for driving the 1.5 kV **HV Source unit**, engineered to provide a secure, stable, and precise source for laboratory testing applications, particularly for Battery Management Systems (BMS) high-voltage measurement inputs
- ❑ Utilizes CAN FD interface
- ❑ Voltage setpoint control:
 - From model
 - Signal chooser



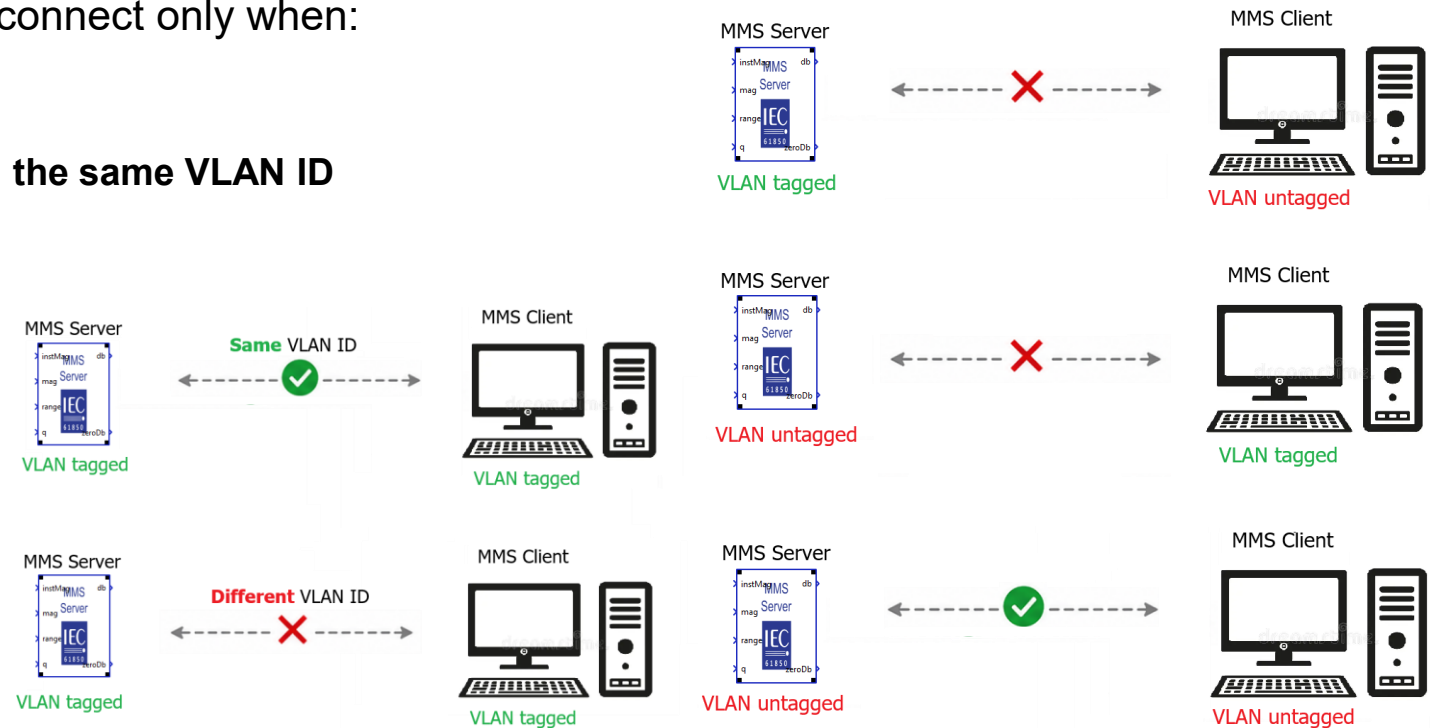
HV Source1



Grid Modernization communication updates

VLAN tagged messages enabled for MMS server

- Configurable **VLAN ID** and **VLAN priority**
- MMS Server and MMS Client will connect only when:
 - They are both **VLAN untagged**
 - They are both **VLAN tagged with the same VLAN ID**



Grid Modernization communication updates

Network parameters configuration for IEC 61850 protocols from SCD files

- ❑ Automatically parse network parameters directly into the component
- ❑ Define network parameters in the **configuration files** and use them on multiple components **without manual configuration**
- ❑ New properties introduced into GOOSE components:
 - APPID
 - MAC Address
- ❑ New properties introduced into MMS Server component:
 - Server port
 - VLAN ID
 - VLAN priority

Component (GOOSE Publisher1) properties

GOOSE Publisher from library 'core'

Configuration should be defined with appropriate configuration file.

Ethernet port: 1

Path to configuration file: typhoon_2servers.scd Choose...

IED: LD

GOOSE Control Block: LD0/LLN0.gcbTEST

MAC Address: [0x01, 0x0C, 0xCD, 0x01, 0x00, 0x24]

APPID: 0x0

Data preview

MMS Server1

File & IED

demo.icd Choose file

Path type: Absolute

Choose IED to simulate: E1

Choose network configuration source: NONE

Path: D:/Workspace/GIT/t_sw/thccc/examples/models/communication protocols/iec 61850 mms server/demo.icd Update configuration: [unchecked]

Network

Ethernet port: 1

Server IP address: 192.168.0.159

Server port: 102

Server Netmask: 255.255.255.0

Server Gateway: [empty]

VLAN

Enable Vlan tagging: [unchecked]

VLAN ID: 0

VLAN priority: 1

Grid Modernization communication updates

Optional fields included for IEC 61850 and IEC 61869 SV Publisher messages

- ❑ Enhanced SV message metadata with:
 - Configurable sample rate and period
 - Additional reference strings
 - Optional UTC timestamp indicating when the sample was acquired

Component (SV Publisher1) properties

SV Publisher from library 'core'

Implements IEC 61850 SV protocol publisher functionality.

General ASDU Signal Quality Faults

svID: pleSVMessage

confRev: 1

Synchronization: static value is: None

gmIdentity: dynamic value is: 0000000000000000

I scaling factor: 1 I type: real

V scaling factor: 1 V type: real

smpRate: ☐ value is: 80

smpMod: ☐ value is: Samples per period (0)

dataSet: ☐ value is:

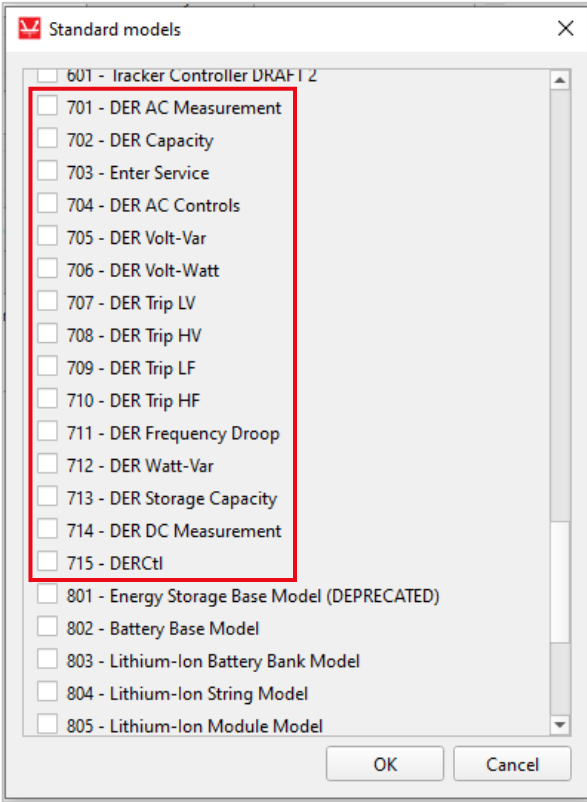
refTime: ☐ value is:

OK Cancel

Grid Modernization communication updates

Support for 700 series models of the SunSpec Modbus standard

- ❑ Support for SunSpec Modbus standard models 701 to 715
- ❑ Series 700 models include configurable repeat counts for nested register groups
 - Allows the number of component inputs and outputs to be adjusted directly from the model configuration dialog

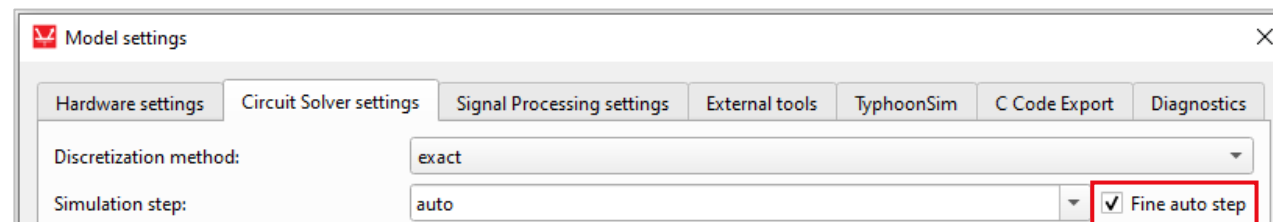


DER Volt-Watt						
	Register	Size	Name	Label	Value	Type
5	40074	1	AdptCrvRslt	Adopt Curve Result	0	enu
6	40075	1	NPt	Number Of Points	2	ui
7	40076	1	NCrv	Stored Curve Count	1	ui
8	40077	2	RvrtTms	Reversion Timeout	0	ui
9	40079	2	RvrtRem	Reversion Time Remaining	0	ui
10	40081	1	RvrtCrv	Reversion Curve	0	ui
11	40082	1	V_SF	Voltage Scale Factor	0	su
12	40083	1	DeptRef_SF	Watt Scale Factor	0	su
13	40084	1	RspTms_SF	Open-Loop Scale Factor	0	su
14	40085	1	ActPt	Crv[1] / Active Points	0	ui
15	40086	1	DeptRef	Crv[1] / Dependent Reference	0	enu
16	40087	2	RspTms	Crv[1] / Open Loop Response Time	0	ui
17	40089	1	ReadOnly	Crv[1] / Curve Access	0	enu
18	40090	1	V	Crv[1] / Pt[1] / Voltage Point	0	ui
19	40091	1	W	Crv[1] / Pt[1] / Dependent Reference	0	in
20	40092	1	V	Crv[1] / Pt[2] / Voltage Point	0	ui
21	40093	1	W	Crv[1] / Pt[2] / Dependent Reference	0	in

UX improvements

“Fine auto” simulation step

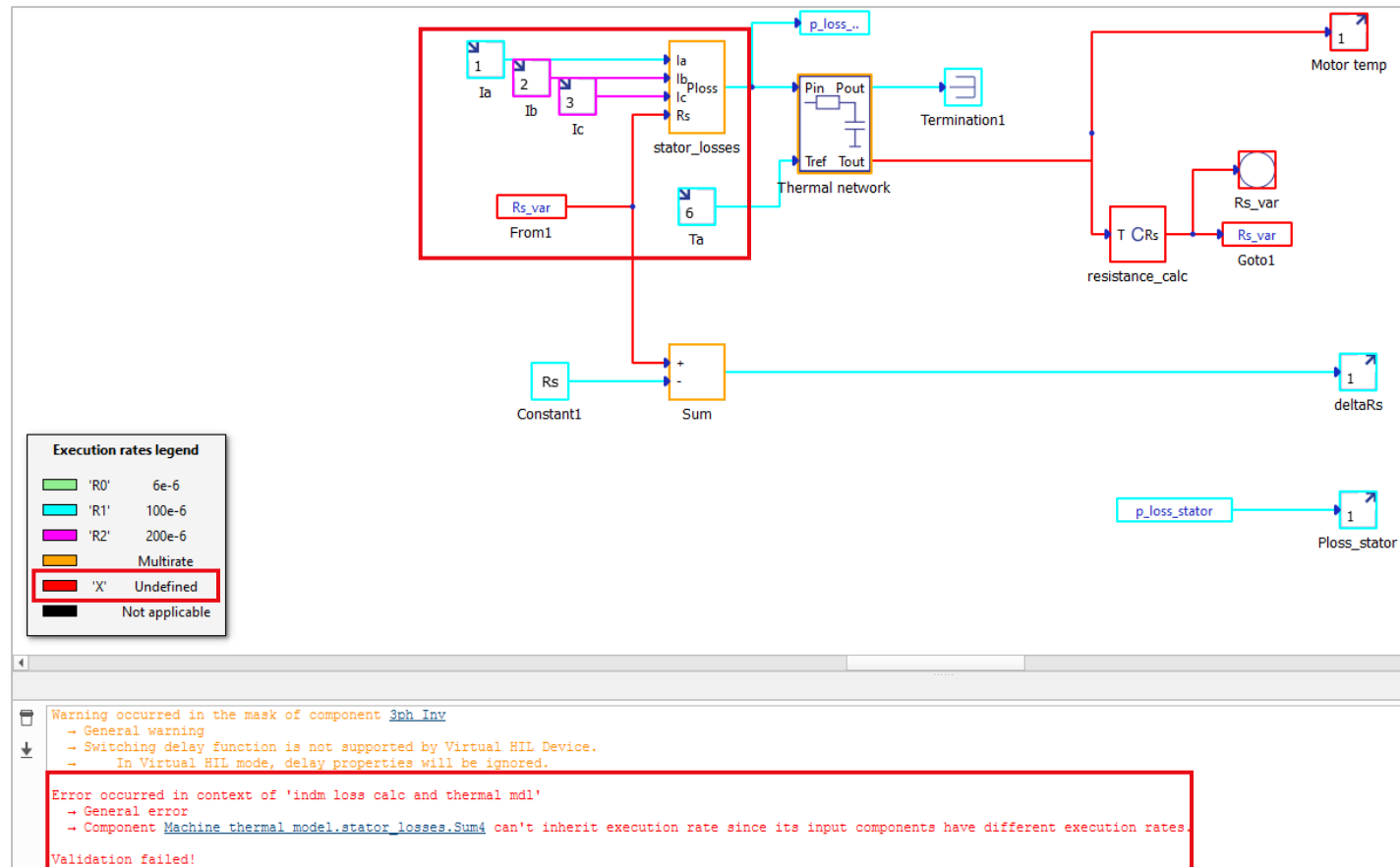
- Added “Fine auto” simulation step option in the model settings window
 - Previously, users could achieve a **50 ns simulation step resolution** only by manually entering the value in the **Simulation Step** text box
 - An option is now available to improve the automatic calculation of the smallest achievable simulation step, enabling it to use **50 ns increments** automatically
 - Applies only to single-HIL models



UX improvements

Visualization of execution rates updated

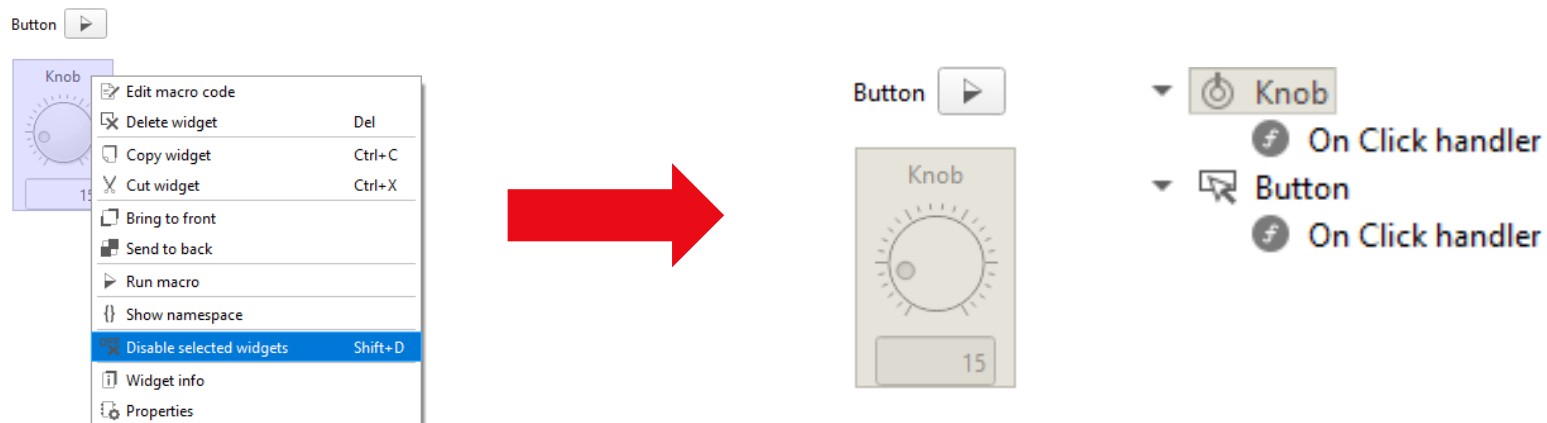
- ❑ Execution rate visualization is now possible even with unsuccessful model validation



UX improvements

Added option to disable SCADA widgets

- ❑ Disabled widgets won't collect any data or execute handlers/macros
 - Certain basic interactions remain available (moving, resizing, copy/cut/paste, modifying parameters within the widget Property dialog)
- ❑ Widget will be visually marked as disabled in HIL SCADA panel and Panel Explorer
- ❑ Disabling widgets can be done by:
 - Using SCADA UI
 - SCADA API (**set_property_value()** function, New **PROP_ENABLED** property)

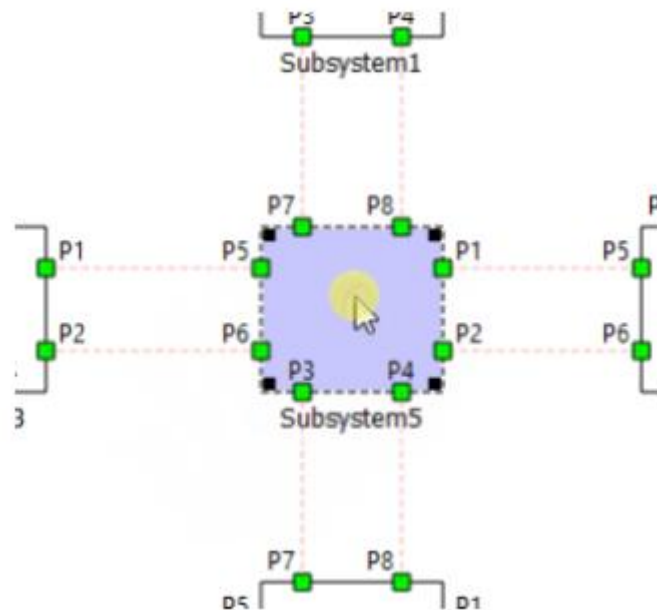


UX improvements

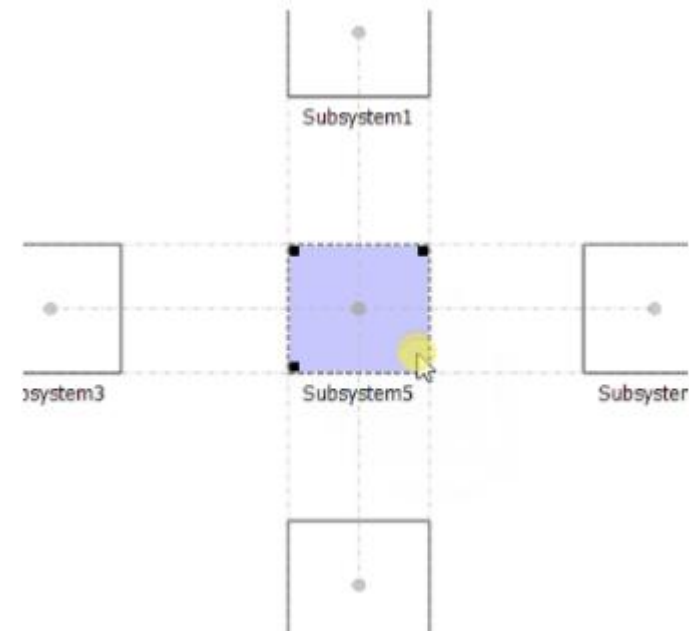
New alignment guidelines

□ New alignment guidelines:

■ Terminal



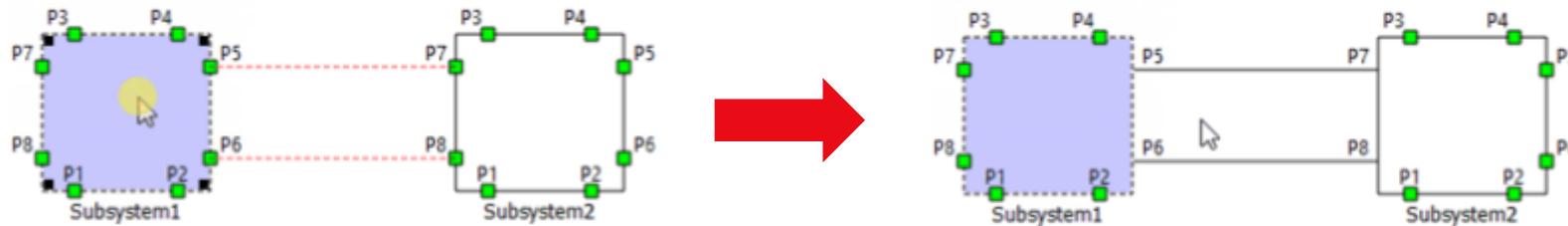
■ Component center



UX improvements

New automated connection types

- Automatically connect components by aligning their ports while holding **Ctrl** and releasing the component once aligned:



- Automatically connect ports by hovering one component's ports over another and dragging:





Thank you for your attention!

